CMOS VLSI CHIP OF NETWORK OF SYNCHRONISED OSCILLATORS: FUNCTIONAL TESTS RESULTS

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Abstract: *This paper presents functional tests results of CMOS VLSI ASIC integrated circuit, which implements a network of synchronised oscillators. The network chip architecture was briefly described. This circuit was designed for segmentation of binary images, which is an important issue in biomedical image analysis. The hardware realisation of oscillator network provides much faster image segmentation compared to computer simulation techniques. Oscillators free frequency tuning idea and procedure have been proposed. Oscillators tunings allowed for segmentation of longer chain objects inputted into synchronised oscillators network chip. Segmentation results of sample binary image obtained using oscillator network chip have been presented and discussed.*

1. Introduction

CMOS VLSI chip of synchronised oscillators' network presented in this paper allows for fast segmentation of binary images. There are many approaches to analysis and labelling of such images. This is a very important aspect of biomedical image analysis, for example in analysis of mast cell microscopic images in dermatology [9]. An approach implemented in discussed network chip is based on "temporary correlation" theory [10], which attempts to explain scene recognition as performed by a human brain. It was demonstrated, that oscillator network which implements this theory, was successfully used for segmentation of Brodatz [1] and biomedical textures. Detailed description of network operation can be found in [10].

Oscillator network is suitable for hardware realisation. A network chip design and simulation results were presented and discussed in [4, 5]. Also, some network functional blocks were described in [6] along with their Spectre simulations results. Some chip functional preliminary tests results have been presented in [7] concluding in necessity of tuning of oscillators frequencies in order to reduce its output duty cycle variability, and in consequence to increment length and number of objects segmented by the network chip.

It was considered, that designed chip was realised as an ASIC (Application Specific Integrated Circuit), to allow combination of both the analogue and the digital technique in a single chip. The circuit was realised in AMIS 0.35µm C035M-D 5M/1P technology by Europractice, and it contains a matrix with 8x8 size.

This paper describes an ASIC CMOS integrated circuit architecture of the oscillator network. The chip block diagram is discussed and oscillators' free frequency tuning idea and procedure are presented. Also, sample binary image segmentation results obtained using the tuned network chip are described and discussed.

2. The chip architecture

A layout of synchronised oscillators network chip is shown in Fig. 1. Layout has been designed using CADENCE version 4.4.6 04/03/2002.

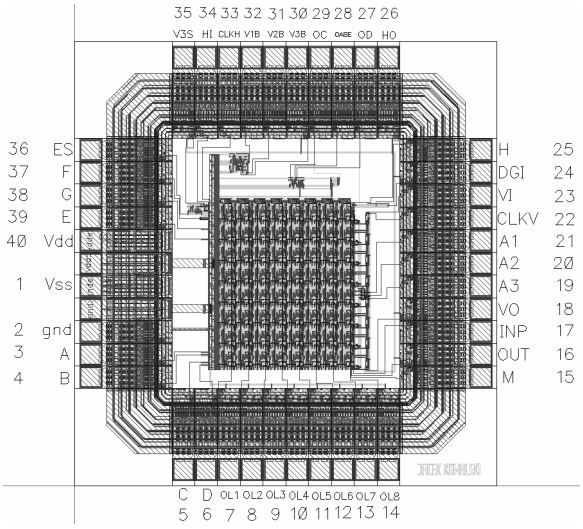


Fig. 1. Layout of synchronised oscillators network chip.

Chip consists of 6368 MOS transistors and occupies 2.29mm^2 of silicon area (1.47mm x 1.55mm). A chip core without pads has the following dimensions: 0.79mm x 0.87mm. The chip has been encapsulated in DIL40

package. Supply current, as measured during image processing is about 1.1mA. The supply voltage is equal to 3V, thus the power consumption is about 3.3mW. The chip works properly with the following range of supply voltages: from 2.4V to 3.6V. A block diagram of processor of synchronised oscillator's network is presented in Fig. 2.

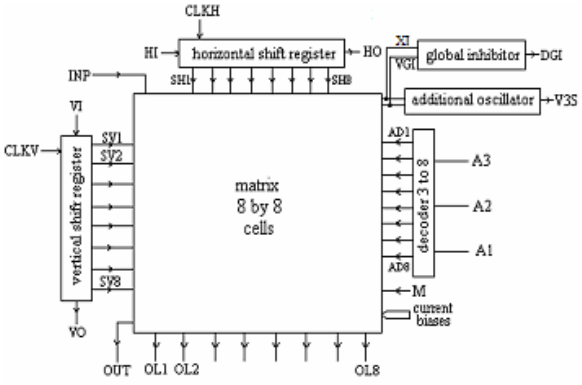


Fig. 2. A block diagram of synchronised oscillators network processor.

The main element of the chip is a matrix 8 by 8 cells, which are processing units of image pixels. Each cell consists of oscillator CMOS circuit, excitatory synapse (network weights), input and output circuits. An image is fed into network chip by serial input INP, pixel by pixel and line by line. Cells are addressed by two shift registers: horizontal and vertical. Shift registers are controlled by two clocks: CLKH and CLKV. Signals HI and VI are used to synchronise image write procedure to the network. Control signals required for loading the input image pixels into a chip are shown in Fig.3.

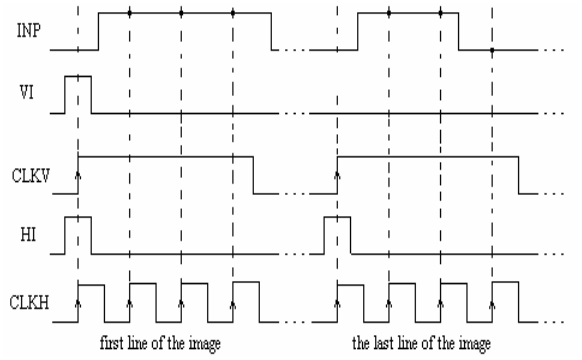


Fig. 3. Control signals required for loading input image into a chip.

Global inhibitor circuit (GI) is connected to all oscillators in the network. DGI is an output digital signal and it is used for observation of global inhibitor activity. An additional oscillator, connected to the whole network by weights, is connected to GI only. This oscillator was implemented to synchronise operation of the oscillator network. It allows also for counting the number of recognised image objects. V3S is an output signal of this oscillator.

The network chip is a mixed signal analogue-digital circuit. Global inhibitor and additional oscillator circuits are fully analogue, matrix of 8 by 8 cells containing oscillators and their additional circuits is analogue in the most part, while shift registers and line decoder are typically digital.

Segmented image objects can be outputted by a serial digital signal OUT. This output is controlled in the same way as input INP by horizontal and vertical registers. It is also possible to observe an activity of selected oscillator's row of the network. This row is addressed by a 3 to 8 decoder. Then, oscillator's states are available in digital outputs OL1-OL8. During network chip testing, a latter described parallel technique was used for observation and analysis of oscillator's outputs.

3. An idea of oscillators tuning

During the first functional chip tests [7] some problems with long chain objects oscillators synchronisation have occurred. This problem is caused by a mismatch in oscillation periods [2,3] in the network. Since oscillator's circuits are analogue, mismatch of MOS transistors [8] causes the mismatch in oscillation frequencies. Some synchronisation improvement can be achieved by increasing a power of excitation synapses weights, which can be realised by increasing current I_F in the chip. This method sometimes is not effective, because causes troubles with desynchronisation of oscillators groups connected to different objects. The best way would be tuning all oscillators to one frequency. In order to adjust free frequencies of oscillators in the network, each oscillator should have possibility of tuning at least one its parameter responsible for frequency separately. Because of a large number of oscillators in the network, implementation of separate tuning circuits and tuning mechanisms can be silicon area consuming and thus expensive. That is why combining image inputting into the network with oscillators tuning seems to be a simplest way to solve this problem.

Tuning procedure can be realised using analogue properties of an input circuit in the oscillator's cell. A schematic of the input pixel value acquisition circuit [5, 6] is shown in Fig. 4.

In each cell the gates of transistors M51 and M52 (nodes SHi, SVi, i=1,…,8, in Fig. 2) are controlled by two shift registers – horizontal register and vertical register. When transistors M51, M52 are switched on, an input cell pixel voltage value is loaded into gate capacitances of M53 and M54 MOS transistors. If at least one of transistors M51, M52 is switched off the pixel voltage value is stored in M53, M54 transistors gate capacitances and this voltage is converted by OTA (transistors M55 – M59) to current. Transistor M57 is working as current source with typical value I_G=1μA. Measured static transfer characteristic $I_{out}(V_{in})$ of input circuit [5] is shown in Fig. 5.

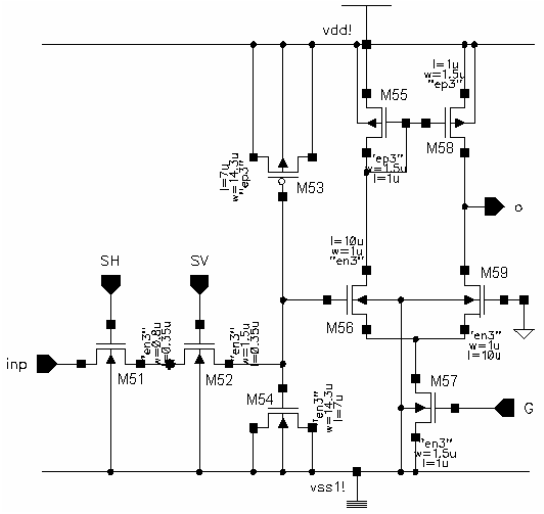


Fig. 4. Schematic of the input circuit.

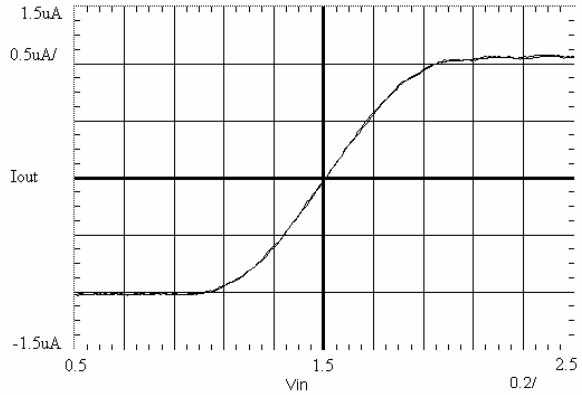


Fig. 5. Measured static transfer characteristic $I_{out}(V_{in})$ of input circuit.

In case of an image inputting without oscillators tuning $I_{out}=I_G$=1μA for image objects and I_{out}=-I_G=-1μA for image background. A transitional part of static transfer characteristic of input circuit was not used so far but it can be used for oscillators frequencies tuning. The following mathematical oscillator model [4, 5, 6] has been used:

$$C_1\frac{dV_1}{dt}=I_A\tanh(aV_1)-I_B\tanh(bV_1)-I_C\tanh(cV_2)-I_E+I_{osc} \quad (1)$$

$$C_2\frac{dV_2}{dt}=I_D\tanh(dV_1)-I_C\tanh(cV_2) \quad (2)$$

where V_1 is an excitatory variable while V_2 is an inhibitory variable. I_A, I_B, I_C, I_D, I_E, C_1, C_2 and a, b, c, d are constants. I_{osc} is a total external stimulation of given oscillator. The following oscillator parameter values were selected: I_A=1.2μA, I_B=2μA, I_C=2μA, I_D=2μA, I_E=2.5μA, a=10, b=2.44, c=2.44, d=500, C_1=15fF, and C_2=1.1pF. For the structure of oscillatory network the total external current excitation I_{osc} of each oscillator is defined by formula (3):

$$I_{osc}=I_{out}+I_F\bigcup_{j=1}^{4}Hev(V_3^j)-I_H\,Hev(DGI)\;;\;Hev(V)=\begin{cases}0 & V<0\\ 1 & V\geq 0\end{cases} \quad (3)$$

where V_3^j is binarised voltage V_1 with a threshold equal to zero of j-th neighbour cell and ⋃ means a logic sum. Typical value of current of weights' polarisation is I_F=0.8μA and current of global inhibitor polarisation I_H=0.22μA. The global inhibitor ensures, that only one oscillator group (representing a given image object) is activated at the same time. A proper selection above parameter values enables to control the network oscillators and provides their appropriate synchronisation and desynchronisation.

In case of an image inputting with oscillators tuning the transitional part of static transfer characteristic of input circuit is used and $I_{out}=I_G\tanh\{g(V_{in}-1.5\text{V})\}$ for image objects and I_{out}=-I_G=-1μA for image background. This means that voltage image pixel value V_{in} for image object can be tuned in order to all oscillators' free frequencies are equal. We can observe in Fig. 5 that maximum current I_{out} tuning range is from 1μA to -1μA and it corresponds to effective input voltage V_{in} from 2V to 1V. For image background V_{in}=0V.

Let us introduce a tuning matrix K as follows:

$$K=\begin{bmatrix}k_{11}&k_{12}&k_{13}&k_{14}&k_{15}&k_{16}&k_{17}&k_{18}\\ k_{21}&k_{22}&k_{23}&k_{24}&k_{25}&k_{26}&k_{27}&k_{28}\\ k_{31}&k_{32}&k_{33}&k_{34}&k_{35}&k_{36}&k_{37}&k_{38}\\ k_{41}&k_{42}&k_{43}&k_{44}&k_{45}&k_{46}&k_{47}&k_{48}\\ k_{51}&k_{52}&k_{53}&k_{54}&k_{55}&k_{56}&k_{57}&k_{58}\\ k_{61}&k_{62}&k_{63}&k_{64}&k_{65}&k_{66}&k_{67}&k_{68}\\ k_{71}&k_{72}&k_{73}&k_{74}&k_{75}&k_{76}&k_{77}&k_{78}\\ k_{81}&k_{82}&k_{83}&k_{84}&k_{85}&k_{86}&k_{87}&k_{88}\end{bmatrix} \quad (4)$$

Then assuming maximum voltage V_{in}=3V, we have for image objects:

$$I_{out\,i,j}=I_G\tanh\{g(3\text{V}\cdot k_{ij}-1.5\text{V})\}\quad i,j=1...8 \quad (5)$$

Oscillators tuning algorithm:

1. Set I_F=0 and I_H=0 in order to oscillators will oscillate without excitatory synaptic connections and without global inhibitor (free oscillations). All oscillators in the network should oscillate. If not, decrease slightly current I_E .
2. Assuming $k_{ij}=1$, i,j=1...8 find oscillator with the smallest frequency f_s of free oscillations.
3. For each oscillator in the network tune its coefficient k_{ij} step by step in order to all oscillators frequencies will be closest to frequency f_s .

Precision of image segmentation by network of synchronised oscillators will depend on precision of above tuning procedure performing. Control signals required for writing the input image pixels into a chip with oscillators frequency tuning are shown in Fig. 6.

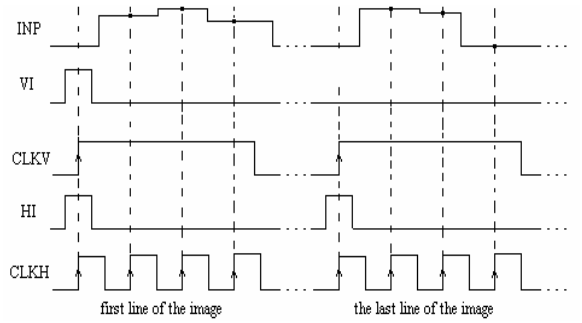


Fig.6. Control signals required for input image loading into a chip with oscillators frequency tuning.

4. Segmentation results of sample binary image using the tuned network chip

In this section, results of a sample of binary image segmentation using the tuned network chip have been described. To perform image segmentation, an experimental laboratory bench was constructed, which is a modified version of that described in [7]. Its block diagram is shown in Fig. 7.

This bench consists of the following elements:

1. PC computer,
2. universal I/O PCI card NI PCI 7831R by National Instruments,
3. special module containing an integrated circuit of oscillator network.

A PC computer working under MS Windows XP and LabView ver. 7.1 software was used to program the NI PCI 7831R card. This I/O card has 96 digital reconfigurable inputs/outputs. Their operating frequency is 40 MHz. The card includes 8 analogue outputs and 8 analog inputs with 16 bits resolution and 1 μs conversion time. This card also contains an internal FPGA structure. 7 card connectors were configured as outputs. They were used to input a binary image to the network chip. There were: CLKH, HI, CLKV and VI. Another 3 inputs were used for addressing one of 8 network rows for oscillator's output reading (signals A1, A2 and A3 in Fig. 2). Another 10 card connectors were configured as inputs. 8 of them (OL1,...,OL8 in Fig. 2) are used for getting the oscillators outputs of a given network row (addressed by A1-A3). Another two are used for reading the states of GI circuit (DGI) and an additional oscillator (V3S). One of analogue PCI card output has been connected through analogue buffer to the chip input INP.

I/O card is connected to a special external test module, which contains a chip with oscillator network. This module is equipped also in I/O buffers (for input and output data and row address) and circuits designed for chip control. There are polarization currents used for setting of oscillator network weights, weight of GI circuit and to control other oscillator parameters (like its characteristics shape [4, 5]). It is also possible to switch on/off an additional oscillator (AO) and global inhibitor (GI) circuits.

The procedure of chip operation for image segmentation was described in [6,7]. Generally, network chip works under control of LabView software which allows to edit/store/read from a hard disk a sample binary image and. Also, the refreshing time can be controlled by this software, which is stored inside of FPGA NI card structure. For oscillator waveforms observation and storage, a logic analyser HP1654B was applied.

Sample binary image used for network chip segmentation is shown in Fig. 8. The refreshing period was set to 1s and an additional oscillator was switched off. Oscillator waveforms obtained for line 1 are presented in Fig. 9a and for line 7 are shown in Fig.9b.

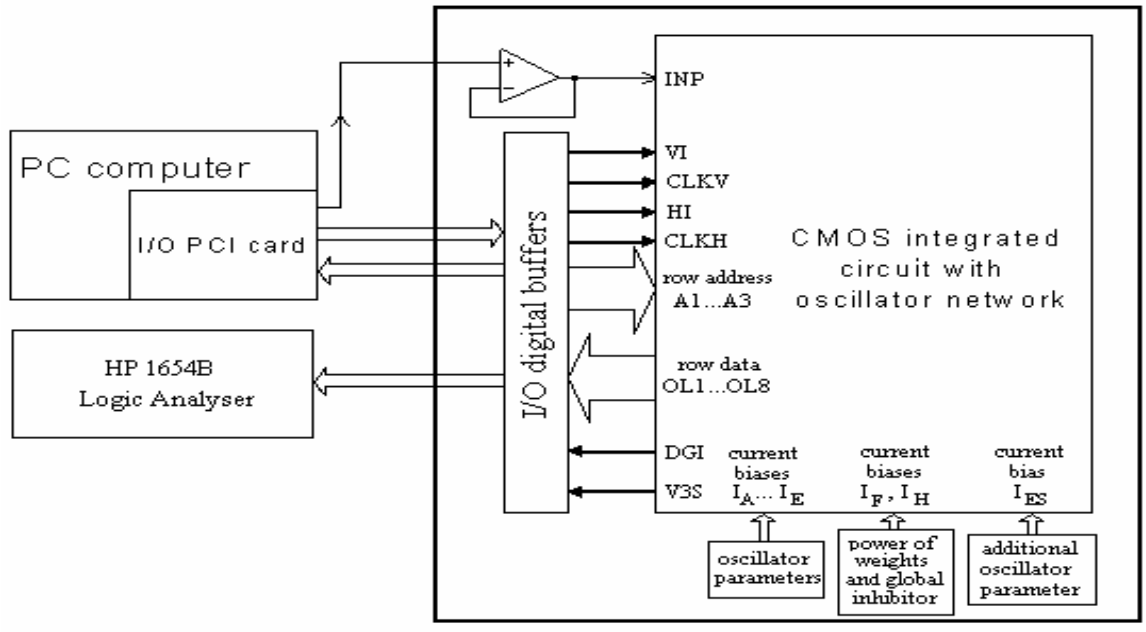


Fig. 7. The block diagram of experimental laboratory bench for binary image segmentation.

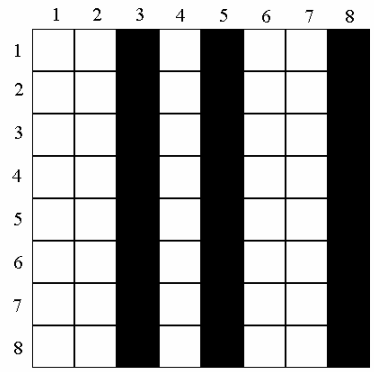
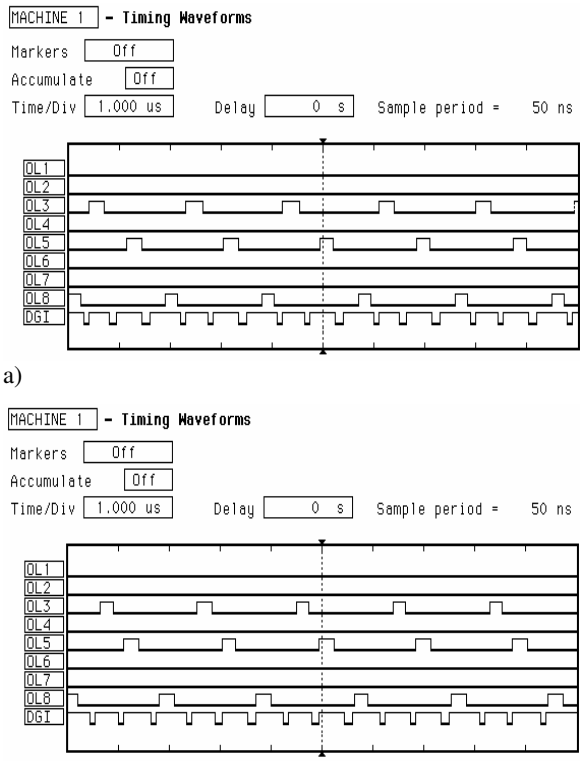


Fig. 8. Sample binary image for segmentation.



a)

b)

Fig. 9. Oscillator waveforms for line 1 (a), for line 7 (b).

Waveforms shown in Fig. 9 do not allow defining the end of image segmentation procedure. To do this, an additional oscillator (AO) should be turned on. Image segmentation results for line 1 with this additional oscillator is shown in Fig. 10.

The additional oscillator can be considered as representing an „extra object". Because network oscillators oscillate continuously, an active state of this additional oscillator indicates the start of segmentation process, which is performed between its active states. Thus, the number of objects detected by the network can be calculated by counting active oscillations between two successive AO active states.

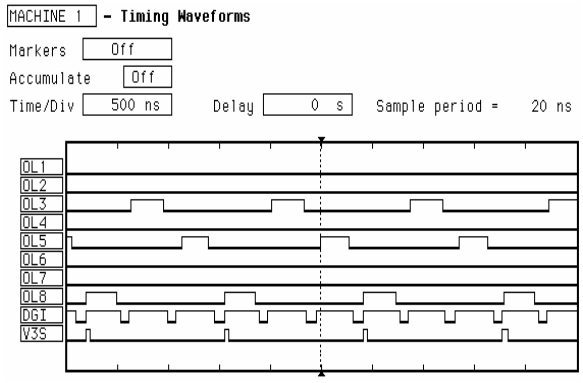


Fig. 10. Oscillator waveforms for line 1 including the additional oscillator.

5. Conclusions

Performed functional tests of integrated circuit implementing oscillators' network shows, that this chip can be used for segmentation of binary images.

The period variability of oscillators outputs resulted by technological mismatch of MOS transistor parameters was a main drawback of the discussed chip. It caused differences in duty cycles of oscillators' outputs, resulting in problems with their synchronisations and thus detection of larger number of objects. This strongly unprofitable phenomenon has been effectively compensated using the oscillators tuning procedure. It resulted in an increment of a length and a number of objects segmented by the network chip. Frequencies of oscillators in the chip were tuning manually so far. Next step is to tune frequencies of oscillators automatically. Universal I/O PCI card NI PCI 7831R can measure frequencies of addressed oscillators and special procedure written in LabView can tune oscillators in the chip. Automatic tuning will be more accurate and much more effective, particularly in case of big dimensions of the network.

Acknowledgements

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